Amendments to the Claims

1. (Currently Amended) A MAC comprising:

at least one PHY-to-MAC port to receive signals indicative of PHY-to-MAC words; and

at least one MAC-to-PHY port to transmit signals indicative of MAC-to-PHY words;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein ~~the~~ a slow mode PHY-to-MAC ~~words~~ word received by the MAC from a PHY ~~include~~ includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

2. (Currently Amended) The MAC as set forth in claim 1, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word.

3. (Original) The MAC as set forth in claim 1, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

4. (Original) The MAC as set forth in claim 1, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

5. (Original) The MAC as set forth in claim 4, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

6. (Currently Amended) The MAC as set forth in claim 4, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

7. (Original) The MAC as set forth in claim 6, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

8. (Currently Amended) A PHY to transmit and receive signals propagated on a medium, and to communicate with a MAC via PHY-to-MAC words and MAC-to-PHY words, the PHY comprising:

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and

at least one PHY-to-MAC port to transmit signals indicative of the PHY-to-MAC words; wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein ~~the~~ a slow mode PHY-to-MAC ~~words~~ word transmitted by the PHY and received by the MAC ~~include~~ includes a transmit cycle field to indicate whether the MAC is requested by the PHY to provide data for transmission on the medium in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

9. (Currently Amended) The PHY as set forth in claim 8, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word.

10. (Original) The PHY as set forth in claim 8, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

11. (Original) The PHY as set forth in claim 8, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

12. (Original) The PHY as set forth in claim 11, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

13. (Currently Amended) The PHY as set forth in claim 11, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

14. (Original) The PHY as set forth in claim 13, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

15. (Currently Amended) A computer system comprising:

a MAC; and

a PHY to receive and transmit signals propagated on a medium and connected to the MAC so that the MAC provides MAC-to-PHY words to the PHY and the PHY provides PHY-to-MAC words to the MAC;

wherein the PHY-to-MAC words and the MAC-to-PHY words are synchronously paired so that the MAC provides one MAC-to-PHY word to the PHY while the PHY provides one PHY-to-MAC word to the MAC;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words having a transmit cycle field;

wherein if the transmit cycle field of a first slow mode PHY-to-MAC word is set to a first value, the first slow mode PHY-to-MAC word being synchronously paired with a first MAC-to-PHY word, then the MAC is requested by the PHY to provide transmit data in a second MAC-to-PHY word for transmission over the medium, where the second MAC-to-PHY word succeeds the first MAC-to-PHY word, and if the transmit cycle field of the first slow mode PHY-to-MAC word is set to a second value different from the first value, then the MAC is requested by the PHY not to include transmit data in the second MAC-to-PHY word ~~no request is made by the PHY to the MAC to provide transmit data~~.

16. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words.

17. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

18. (Original) The computer system as set forth in claim 15, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

19. (Original) The computer system as set forth in claim 18, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

20. (Original) The computer system as set forth in claim 18, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words; and

the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

21. (Original) The computer system as set forth in claim 20, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit

position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

A1 end